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Display device

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Display device

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The invention relates to a display device comprising a liquid crystal material between a first substrate provided with row or selection electrodes and a second substrate provided with column or data electrodes, in which overlapping parts of the row and column electrodes define picture elements, drive means for driving the column electrodes in conformity with an image to be displayed, and drive means for driving the row electrodes.

Such display devices are used in, for example, portable apparatuses such as laptop computers, notebook computers and telephones.

Passive-matrix displays of this type are generally known and are generally driven by providing the row or selection electrodes with selecting voltages and simultaneously supplying data voltages to the column or data electrodes as described by Alt & Pleshko in IEEE Trans El. Dev. Vol. ED –21, No. 2, Feb 1974, pp146 –155. For realizing a high number of lines, passive-matrix displays are increasingly based on the STN (Super-Twisted Nematic) effect. An article by T.J. Scheffer and B. Clifton "Active Addressing Method for High- Contrast Video Rate STN Displays", SID Digest 92, pp. 228-231 describes how the phenomenon of "frame response" which occurs with rapidly switching liquid crystal materials is avoided by making use of "Active Addressing". In this method, all rows are driven throughout the frame period with mutually orthogonal signals, for example, Walsh functions. The result is that each picture element is continuously excited by pulses (in an STN LCD of 240 rows: 256 times per frame period) instead of once per frame period. In "multiple row addressing" or MRA, a (sub-) group of p rows is driven with mutually orthogonal signals.

Display cells based on the STN (Super-Twisted Nematic) effect generally have a very steep transmission voltage characteristic, which makes it difficult to realize gray levels. One method is sub-pixellation which goes at the cost of the maximum number of lines. Another method is "frame rate control" (FRC) which is a technique to generate different gray values by varying the state of a picture element between ON and OFF within a certain number of consecutive frame periods.

In this respect a frame period is the period in which all rows are selected one time, be it separately (Alt & Pleshko) or in groups (MRA). Thanks to the persistency of the human vision system and the properties of the liquid crystal, the different states are averaged and perceived as one gray value.

If the number of gray levels within a grayscale increases however the number of consecutive frame periods (which is also called a super-frame in this Patent Application) increases too, leading to flicker.

It is, inter alia, an object of the invention to provide a display device of the type described above, in, which minimal flickering occurs.

A further purpose of the invention is to provide a display device of the type described above in which the power used is lowered with respect to existing devices.

To this end a device according to the invention has drive means comprising means for driving a group of picture elements during time periods within a sequence of time periods, the driving of different picture elements within a sequence of time periods being phase-shifted with respect to each other

A phase in this Patent Application is understood to be the number of a sub-selection period in a sequence of time periods, when considering the total number of sequences, in this case the number of the position of the phase in a super-frame. In fact it specifies the (sub)-selection period at which a picture element or a group of picture elements is selected. Similar remarks apply to selecting a picture element or a group of picture elements during selection of a sub-selection time in subsequent sequences of selection times.

The invention is based inter alia on the insight that non-sequential selections of time periods within a sequence of time periods leads to different periodical driving (or even non-periodical driving) of different picture elements. The human vision system more easily averages different states now, which are perceived as one gray value.

The phase shifting may be altered after each sequence of time periods.

On the other hand the invention is based on the insight that using a special grayscale table may diminish the number of voltage transitions in a driver. A special embodiment of the invention therefore comprises a grayscale table for generating graylevel data in which grayscale table sequences of s (s >1) sequential graylevels are defined by grouping s sequential graylevels within a sequence, said sequences being allotted to non-sequential selections of time periods within a sequence of time periods.

In this case preferably (s-1) increases (or decreases) of the number of selections within a sequence of selections are allotted to one time period only. Said time period may comply with a frame period in which a sequence of time periods is a sequence of frame periods.

A preferred embodiment of a device according to the invention in this case comprises means to change the frame-phase of a frame during selection of said frame in subsequent sequences of frame periods.

These and other aspects of the invention will now be elucidated with reference to an embodiment and the drawings in which

Figure 1 shows an electric equivalent circuit diagram of a part of a display device in which the invention is used,

Figure 2 shows selection and data voltages for a display device according to Figure 1,

Figure 3 shows a set of picture elements having certain gay-levels

Figure 4 schematically shows one way of driving these picture elements to display said gray-levels, while

Figure 5 shows an electric equivalent circuit diagram of a part of another display device in which the invention is used and

Figures 6 and 7 show selection and data voltages for a display device according to Figure 5.

The Figures are diagrammatic and not drawn to scale. Corresponding elements are generally denoted by the same reference numerals.

Figure 1 is an electric equivalent circuit diagram of a part of a display device 1 to which the invention is applicable. It comprises a matrix of picture elements 8 defined by the areas of crossings of m row or selection electrodes 7 and n column or data electrodes 6. The row electrodes, in one mode of driving, are consecutively selected by means of a row driver 4, while the column electrodes are provided with data via a data register 5. To this end, incoming data 2 are first processed, if necessary, in a processor 3. Mutual synchronization between the row driver 4 and the data register 5 takes place via drive lines 9.

A first method to drive the display device 1 by selecting all rows sequentially (or non-sequentially) by selecting one line at a time (Alt & Pleshko addressing). The period over which all line are selected is called a frame (time). Using multiple frames it is possible to generate gray-levels. The number of frames in which a grayscale is defined is indicated as a superframe. Table 1 shows a superframe consisting of 4 frames in which 5 gray-levels can be generated.

gray-level	frame 1	frame 2	frame 3	frame 4
GS 0	off	off	off	off
GS 1	on	off	off	off
GS 2	on	off	on	off
GS 3	on	on	on	off
GS 4	on	on	on	on

Table 1

In fact Table 1 defines a grayscale table for generating graylevel data in which grayscale table sequences of s ($s = 5$) sequential graylevels are defined by grouping the graylevels within the sequence of time periods (a superframe) as shown (and with 16 frames basically 17 gray values could be generated). If such graylevels are kept constant for a certain longer time period different picture elements are driven by a driver which repeats these superframes, as shown in Table 2

gray-level	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4
	Superframe 1				Superframe 2				Superframe 3			
GS 0	off	off	off	off	off	off	off	off	off	off	off	off
GS 1	on	off	off	off	on	off	off	off	on	off	off	off
GS 2	on	off	on	off	on	off	on	off	on	off	on	off
GS 3	on	on	on	off	on	on	on	off	on	on	on	off
GS 4	on	on	on	on	on	on	on	on	on	on	on	on

Table 2

To obtain GS 3 in e.g. four picture elements (pixels) the driving would be:

	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4
	Superframe 1				Superframe 2				Superframe 3			
pixel 0	on	on	on	off	on	on	on	off	on	on	on	off
pixel 1	on	on	on	off	on	on	on	off	on	on	on	off
pixel 2	on	on	on	off	on	on	on	off	on	on	on	off
pixel 3	on	on	on	off	on	on	on	off	on	on	on	off

Table 2'

Since for all grayvalues the same superframes are time -sequentially repeated this leads to noticeable flickering. To avoid this, according to the invention a mixing technique is used. For example to obtain GS 3 in stead of switching the picture element off during the last out of the four consecutive frames as depicted in Table 2, different (neighboouring) picture elements (pixels) are switched off in the fourth, first and second frame for the different picture elements respectively (Table 3). Since in total, there exist four different patterns to generate GS 3 with four frames in one superframe resulting in:

gray-level 3	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4	fr 1	fr 2	fr 3	fr 4
	Superframe 1				Superframe 2				Superframe 3			
pixel 0	on	on	on	off	on	on	on	off	on	on	on	off
pixel 1	on	on	off	on	off	on	off	on	on	on	off	on
pixel 2	on	off	on	on	on	off	on	on	on	off	on	on
pixel 3	off	on	on	on	off	on	on	on	off	on	on	on

Table 3

So in this example time periods comply with a frame period in which a sequence of time periods is a sequence of frame periods within a sequence of time periods (within a superframe). According to the inventionthe driving of different picture elements within a sequence of time periods (a superframe) is phase-shifted over one frame period time period relative to each other for different pixels (a phase in this example corresponding to a frame). The phase shifting may be altered after each sequence of time periods (superframe).

Another way to generate graylevels is to split the line time for the column signal. Figure 2 shows a line time split into 4 parts (indicated as sub-line times), which also results in 5 graylevels, while a phase in this example corresponds to a sub-line time. Combining the principle of line time splitting with the principle as described with respect to Tables 1, 2 opens the possibility of generating 17 gray-levels (GS0 –GS16), as shown in Table 4

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3
GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
GS4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GS5	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
GS6	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
GS7	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
GS8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
GS9	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
GS10	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
GS11	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
GS12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
GS13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
GS14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
GS15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
GS16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 4

The driving of different picture elements within a sequence of time periods according to the invention is phase-shifted over one frame period time period within two sequential superframes again (a phase now corresponding to a sub-line time). According to the invention the phase shifting is altered after each sequence of time periods (superframe), which implies for example the following driving in the next superframe (Table 5)

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	$P0_{00}$	$P1_{00}$	$P2_{00}$	$P3_{00}$	$P1_{01}$	$P2_{01}$	$P3_{01}$	$P0_{01}$	$P2_{02}$	$P3_{02}$	$P0_{02}$	$P1_{02}$	$P3_{03}$	$P0_{03}$	$P1_{03}$	$P2_{03}$
GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
GS4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GS5	1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
GS6	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
GS7	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
GS8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
GS9	1	1	1	1	1	1	1	1	0	0	0	1	0	0	0	0
GS10	1	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0
GS11	1	1	1	1	1	1	1	1	1	0	1	1	0	0	0	0
GS12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
GS13	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0
GS14	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0
GS15	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
GS16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 5

In said Table the sub-line times (pulses) are indicated as $\mathbf{P1_{00}}$ or $\mathbf{Pp_{xy}}$, in which p is the phase number of the gray-table in Table 4, x refers to the first gray-table definition (as defined in Table 4) as used in the first superframe and y refers to the frame-number in the superframe. So in short the next superframe is defined, supposing a cyclical phase-sequence by:

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	$P1_{00}$	$P2_{00}$	$P3_{00}$	$P0_{00}$	$P2_{01}$	$P3_{01}$	$P0_{01}$	$P1_{01}$	$P3_{02}$	$P0_{02}$	$P1_{02}$	$P2_{02}$	$P0_{03}$	$P1_{03}$	$P2_{03}$	$P3_{03}$

And the next-following superframe by:

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	$P2_{00}$	$P3_{00}$	$P0_{00}$	$P1_{00}$	$P3_{01}$	$P0_{01}$	$P1_{01}$	$P2_{01}$	$P0_{03}$	$P1_{02}$	$P2_{02}$	$P3_{02}$	$P1_{03}$	$P2_{03}$	$P3_{03}$	$P4_{03}$

So depending on the kind of driving (based on time periods or sub-line times (pulses) in frame periods) a grayscale-table is defined which is used in driving the display device.

When using a superframe, consisting of 16 frames, each having 4 sub-line times, and driving 2 lines simultaneously as in multiple row addressing, certain picture elements are for example allotted to columns and rows as in the matrix shown below.

	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7	——	C_128	C_129	C_130	C_131
R_0	0	5	13	11	0	5	13	11	——	0	5	13	11
R_1	4	10	2	7	4	10	2	7	——	4	10	2	7
R_2	0	5	13	11	0	5	13	11	——	0	5	13	11
R_3	4	10	2	7	4	10	2	7	——	4	10	2	7
-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-
R_128	0	5	13	11	0	5	13	11	——	0	5	13	11
R_129	4	10	2	7	4	10	2	7	——	4	10	2	7
R_130	0	5	13	11	0	5	13	11	——	0	5	13	11
R_131	4	10	2	7	4	10	2	7	——	4	10	2	7

Table 6

Each picture element in the matrix (132 rows, 132 columns) has a particular phase (frame number, which is indicated per picture element) which corresponds to a particular frame by which the picture element is driven. The phases are repeated in blocks of 2 rows and 4 columns (2 x 4 mixing). The same frame drives each picture element in successive superframes, comparable to the driving shown in Table 2 (see Table 7).

super frame												
frame 0				frame 1				——	frame 15			
0	5	13	11	0	5	13	11	——	0	5	13	11
4	10	2	7	4	10	2	7	——	4	10	2	7
0	5	13	11	0	5	13	11	——	0	5	13	11
4	10	2	7	4	10	2	7	——	4	10	2	7

Table 7

According to the invention, in a similar way as described above, the particular phase (frame number) is now increased after each frame time, leading to the following driving scheme:

super frame												
frame 0				frame 1				----	frame 15			
0	5	13	11	1	6	14	12	----	15	4	12	10
4	10	2	7	5	11	3	8	----	3	9	1	6
0	5	13	11	1	6	14	12	----	15	4	12	10
4	10	2	7	5	11	3	8	----	3	9	1	6

Table 8

To display a block of (4 x 4) picture elements of the display, as shown in Figure 3, having picture elements 8 in the upper half displayed in gray-level 7 (GS 7), while the lower part is displayed in gray-level 9 (GS 9).
Suppose GS 7 and GS 9 are defined according to Table 9. In which Fp defines a frame (part) (which may be a frame as part of a superframe, like in Tables 2,3 or a phase as part of a frame, like in Tables 4, 5).

Frame (part)	Fp0	Fp1	Fp2	Fp3	Fp4	Fp5	Fp6	Fp7	Fp8	Fp9	Fp 10	Fp 11	Fp 12	Fp 13	Fp 14	Fp 15
GS7	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
GS9	0	1	1	0	1	1	0	1	0	1	1	0	1	1	0	1

Table 9.

The '1' represents an on frame (part), a zero corresponds to an off frame (part)
According to the phases given in Table 8 the picture elements are in the on (black) and off (white) state respectively as indicated in Figure 4. For example, a picture element 8(1) displaying gray-level GS 7 is in the on state during phase 0 ($\mathbf{Fp0_{00}}$) of frame 0 (frame (part) 0). More generally the notation $\mathbf{Fpx_{yy}}$ is used in which x refers to the frame, while yy refers to the phase.

Other picture elements 8 (2, 3, 4) displaying gray-level GS 7 are driven during the other phases (5, 13, 11 or $\mathbf{Fp0_{05}}$, $\mathbf{Fp0_{13}}$, $\mathbf{Fp0_{11}}$) of frame 0 (frame (part)s 5, 13, 11) in the off state. In a similar way picture elements 8 (5, 6, 7) displaying gray-level GS 7 are driven in the on state during phases 4, 10, 2 or $\mathbf{Fp0_{04}}$, $\mathbf{Fp0_{10}}$, $\mathbf{Fp0_{02}}$ of frame 0 (frame (part) 0). The picture elements 8 (8) displaying gray-level GS 7 is driven in the off state by phase 7($\mathbf{Fp0_{07}}$) of frame 0 (frame (part) 7).

In a similar way to obtain gray-level GS 9 picture elements 8 (10, 11, 13, 14, 15, 16) displaying gray-level GS 9 are driven in the on state during phases 5, 13, 4, 10, 2 and 7 or $\mathbf{Fp0}_{05}$, $\mathbf{Fp0}_{13}$, $\mathbf{Fp0}_{04}$, $\mathbf{Fp0}_{10}$, $\mathbf{Fp0}_{02}$ and $\mathbf{Fp0}_{07}$ of frame 0 (frame (part)s 5, 13 , 4, 10, 2, 7) and picture elements 8 (9, 12) are driven in the off state by phases 0, 11 or $\mathbf{Fp0}_{00}$, $\mathbf{Fp0}_{11}$ of frame 0 (frame (part)s 0, 11).

In the next frame the phase-numbers (frame (part)numbers) are increased by one. Based on the on (black) and off (white) states respectively as indicated in Table 9 the picture element 8(1) displaying gray-level GS 7 is in the off state during phase 0 ($\mathbf{Fp1}_{00}$) of frame 1 (frame (part) 1). Other picture elements 8 (2, 3, 4) displaying gray-level GS 7 are driven during the other phases (6, 14, 12) or $\mathbf{Fp1}_{06}$, $\mathbf{Fp1}_{14}$, $\mathbf{Fp1}_{12}$ of frame 1 (frame (part)s 6, 14, 12) in the on state. In a similar way picture elements 8 (5, 6, 7) displaying gray-level GS 7 are driven in the off state during phases 5, 11, 3 or $\mathbf{Fp1}_{05}$, $\mathbf{Fp1}_{11}$, $\mathbf{Fp1}_{13}$ of frame 1 (frame (part) 1). The picture elements 8 (8) displaying gray-level GS 7 is driven in the off state by phase 8 ($\mathbf{Fp1}_{08}$) of frame 1 (frame (part) 8), see Figure 4.

In a similar way to obtain gray-level GS 9 picture elements 8 (10, 11, 14, 15, 16) displaying gray-level GS 9 are driven in the off state during phases 6, 14, 11, 3 and 8 or $\mathbf{Fp1}_{06}$, $\mathbf{Fp1}_{14}$, $\mathbf{Fp1}_{11}$, $\mathbf{Fp1}_{03}$ and $\mathbf{Fp1}_{08}$ of frame 1 (frame (part)s 6, 14, 11, 3, 8) and picture elements 8 (9, 12, 13) are driven in the on state by phases 1, 12 and 5 or $\mathbf{Fp1}_{01}$, $\mathbf{Fp1}_{12}$, $\mathbf{Fp1}_{05}$ of frame 1 (frame (part)s 1, 12, 5) , see Figure 4.

By defining of the grayscale (levels) according to Table 9 on and off frames are spread over the superframe as much as possible. This makes that the effective voltage (or root mean square Voltage V_{rms}) which the liquid crystal layer encounters is spread evenly over the superframe thereby suppressing flicker and enabling low frame frequencies. Since adjacent picture elements having substantially the same gray levels are addressed out of phase the invention enables lowering of the frame frequency. For picture elements addressed in phase (prior art) frequency flicker is visible at a certain frequency whereas at this same frame frequency flicker is not visible in case picture elements are addressed out of phase.

In stead of using Table 5 for defining the gray-levels, other definitions may be used as well e.g. the driving as shown in Table 5 may be used as gray-levels defined as initial gray-levels. Another possibility in which grayscale table sequences of s (s =4) sequential graylevels are defined by grouping s sequential graylevels within a sequence is shown below.

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3
GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS2	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS3	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
GS4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GS5	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
GS6	1	1	1	1	0	0	0	0	1	1	0	0	0	0	0	0
GS7	1	1	1	1	0	0	0	0	1	1	1	0	0	0	0	0
GS8	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
GS9	1	1	1	1	1	0	0	0	1	1	1	1	0	0	0	0
GS10	1	1	1	1	1	1	0	0	1	1	1	1	0	0	0	0
GS11	1	1	1	1	1	1	1	0	1	1	1	1	0	0	0	0
GS12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
GS13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
GS14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
GS15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
GS16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 10

Some other possibilities are e.g.:

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3
GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
GS2	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
GS3	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
GS4	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
GS5	1	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0
GS6	1	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0
GS7	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0
GS8	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
GS9	1	1	1	1	1	1	1	1	0	0	0	0	1	0	0	0
GS10	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0	0
GS11	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1	0
GS12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
GS13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
GS14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
GS15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
GS16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 11

Or

frame	Frame 0				Frame 1				Frame 2				Frame 3			
pulse	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3	P0	P1	P2	P3
GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
GS2	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
GS3	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
GS4	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
GS5	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	0
GS6	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	0
GS7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	0
GS8	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
GS9	1	1	1	1	0	0	0	0	1	1	1	1	1	0	0	0
GS10	1	1	1	1	0	0	0	0	1	1	1	1	1	1	0	0
GS11	1	1	1	1	0	0	0	0	1	1	1	1	1	1	1	0
GS12	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0
GS13	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
GS14	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
GS15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
GS16	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Table 12

Figure 5 shows a display device in which multiple row addressing is applied as described in an article by T.J. Scheffer and B. Clifton "Active Addressing Method for High-Contrast Video Rate STN Displays", SID Digest 92, pp. 228-231, which describes how the phenomenon of "frame response" which occurs with rapidly switching liquid crystal materials is avoided by making use of "Active Addressing". In this method, all rows are driven throughout the frame period with mutually orthogonal signals, for example, Walsh functions. The result is that each picture element is continuously excited by pulses (in an STN LCD of 240 rows: 256 times per frame period) instead of once per frame period. In "multiple row addressing", a (sub-)group of p rows is driven with mutually orthogonal signals. Since a set of orthogonal signals, such as Walsh functions, consists of a plurality of functions which is a power of 2, i.e. 2^S, p is preferably chosen to be equal thereto as much as possible, i.e. generally $p = 2^S$ (or also $p = 2^S$-1). The orthogonal row signals $F_i(t)$ are preferably square-wave shaped and consist of voltages $+F$ and $-F$, while the row voltage is equal to zero outside the selection period. The elementary voltage pulses from which the orthogonal signals are built up are regularly distributed across the frame period. In this way, the picture elements are then excited 2^S (or (2^s-1)) times per frame period with regular intermissions instead of once per frame period. Even for low values of p such as $p = 3$ (or 4) or $p = 7$ (or 8) the frame response appears to be suppressed just as satisfactorily as when driving all rows simultaneously, such as in "Active Addressing", but it requires much less electronic hardware.

The display device of Figure 5 comprises again a matrix 11 of picture elements at the area of crossings of m rows 12 and n columns 13 which are provided as row and column electrodes on facing surfaces of substrates 14, 15, as can be seen in the cross-section shown in the matrix 11. The liquid crystal material 16 is present between the substrates. Other elements such as orientation layers, polarizers, etc. are omitted for the sake of simplicity in the cross-section.

The device further comprises a row function generator 17 in the form of, for example, a ROM for generating orthogonal signals $F_i(t)$ for driving the rows 12. Similarly as described in said article by Scheffer and Clifton, row vectors driving a group of p rows via drive circuits 4 are defined during each elementary time interval. The row vectors are written into a row function register 19.

Information 10 to be displayed is stored in a nxm buffer memory 11 which contains a look up table 20, for example derived as discussed above with rrespect to Figure 3

(combination of the Tables 8,9) and read as information vectors per elementary unit of time. Signals for the column electrodes 6 are obtained by multiplying the then valid values of the row vector and the information vector during each elementary unit of time and by subsequently adding the obtained products. The multiplication of the values which are valid during an elementary unit of time of the row and column vectors is realized by comparing them in an array 22 of m exclusive ORs. The addition of the products is effected by applying the outputs of the array of exclusive ORs to the summing logic 13. The signals 21 from the summing logic 13 drive a column drive circuit 5 which provides the columns 3 with voltages $G_j(t)$ having $p+1$ possible voltage levels. Every time, p rows are driven simultaneously, in which $p < N$ ("multiple row addressing"). The row vectors therefore only have p elements, as well as the information vectors, which results in a saving of the required hardware such as the number of exclusive ORs and the size of the summing circuit, as compared with the method in which all rows are driven simultaneously with mutually orthogonal signals ("Active Addressing").

The drive electronics is minimized by choosing p to be low, for example, in the range between 3 and 8. Fig. 6 shows schematically how the display device is driven with a set of orthogonal functions referred to as $F_i(t)$ and the pulse patterns derived therefrom for the purpose of multiple row addressing with $p = 4$ for a first frame.

As one possible example it is shown how gray levels can be displayed using this set of orthogonal functions according to the grayscale definition of Table 10.

The orthogonal functions or row selection pulses are indicated schematically. The general formula calculating the column signals G(t) for p rows addressed simultaneously is given by:

$$G_i(t) = C \sum_{i=1}^{p} d_{ij} F_i(t)$$

where $F_i(t)$ represents the orthogonal function applied to row_i and d_{ij} represents the picture element data of row_i and $column_j$.

For above example we have:

$$G_1(t) = C \{d_{11}F_1(t) + d_{21}F_2(t) + d_{31}F_3(t) + d_{41}F_4(t)\}$$

According to Table 10 GS 6 is defined as having all 4 sub-line times in the on state for frame 0, i.e. d_{11} is -1 for 4 sub-line times (= one line time). For GS 3 the picture element is in the on

state for the first 3 sub-line times and the 4th sub-line time the picture element is in the off state, i.e. d_{21} is –1 for the first 3 sub-line times and +1 for the 4th line time. For GS 11 the picture element is in the on state for all four sub-line times, while for GS 0 the picture element is in the off state for all four sub-line times.

Function $F_1(t)$ is –1 for the first line time (i.e. 4 sub-line times), +1 for the 2nd, 3rd and 4th line time. Function $F_2(t)$ is –1 for the second line time (i.e. 4 sub-line times), +1 for the first , 3rd and 4th line time etcetera.

Substituting this for the first 4 line times of frame 0 find the column signal G1(t) for column 1 as shown in Figure 7 is found.

The invention is of course not limited to the embodiments shown. The logic in the driver IC can make multiple selections from the programmed orthogonal matrices during frames and also after whole frames. Also vectors within an orthogonal matrix can be swapped or inverted by the driver to reduce the number of column signal transitions. Furthermore it is possible to let the driver IC decide which orthogonal matrix it will use for certain display data content. In this way an adaptive multiple orthogonal matrix multiple row addressing drive is created which results in low display current and module power independent of the data to be displayed.

The protective scope of the invention is not limited to the embodiments described. The invention resides in each and every novel characteristic feature and each and every combination of characteristic features. Reference numerals in the claims do not limit their protective scope. The use of the verb "to comprise" and its conjugations does not exclude the presence of elements other than those stated in the claims. The use of the article "a" or "an" preceding an element does not exclude the presence of a plurality of such elements.

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CLAIMS:

1. A display device comprising a liquid crystal between a first substrate provided with row or selection electrodes and a second substrate provided with column or data electrodes, in which overlapping parts of row and column electrodes define picture elements, drive means for driving the column electrodes in conformity with an image to be displayed, and drive means for driving the row electrodes which, in the operating condition, within a sequence of m ($m > 1$) time periods, during each time period sequentially supply groups of p ($p \geq 1$) row electrodes during a selection time with mutually orthogonal selection signals for driving picture elements, the drive means comprising means for driving a group of picture elements during time periods within a sequence of time periods, the driving of different picture elements within a sequence of time periods being phase-shifted with respect to each other.

2. A display device as claimed in claim 1 in which the phase numbers of the time periods are increased or decreased by one after each sequence of time periods.

3. A display device as claimed in claim 1 or 2 comprising a grayscale table for generating graylevel data in which grayscale table sequences of s ($s > 1$) sequential graylevels are defined by grouping s sequential graylevels within a sequence, said sequences being allotted to non-sequential selections of time periods within a sequence of time periods.

4. A display device as claimed in claim 3 in which a sequence of selections is allotted to increasing gray values or decreasing gray values.

5. A display device as claimed in claim 4 in which (s-1) increases (or decreases) of the number of selections within a sequence of selections is allotted to one time period only.

6. A display device as claimed in claim 1 in which a sequence of time periods is a sequence of frame periods.

7. A display device as claimed in claim 6 comprising means to change the frame-phase of a frame during selection of said frame in subsequent sequences of frame periods.

8. A display device as claimed in claim 1 comprising means to provide during sub-selection times of a selection time different voltages to the column electrodes.

9. A display device as claimed in claim 1 comprising means to change the sub-selection time-phase during selection of a sub-selection time in subsequent sequences of selection times.

10. A display device as claimed in claim 1, the phase shifting being altered after each sequence of time periods.

11. A display device as claimed in claim 1 or 2 in which $p = 1$.

12. A display device as claimed in claim 5 in which $p = 1$ the drive means for driving the column electrodes having means for providing different voltages to the column or data electrodes at sub-selection times of the selection times.

13. A display device as claimed in claim 1 or 2 in which $p = 4$.

ABSTRACT:

In RMS driving (both Alt & Pleshko and MRA addressing) of passive matrix devices flicker and power are reduced by driving groups of picture elements during time periods within a sequence of time periods while the driving of different picture elements within a sequence of time periods is phase-shifted over at least one time period, while the phase shifting is altered after each sequence of time periods.

Fig. 1

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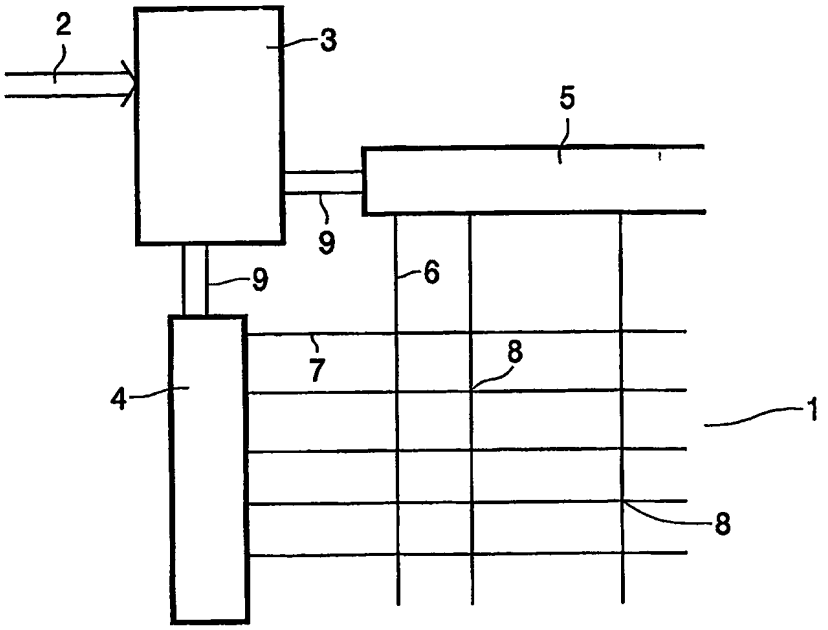

FIG. 1

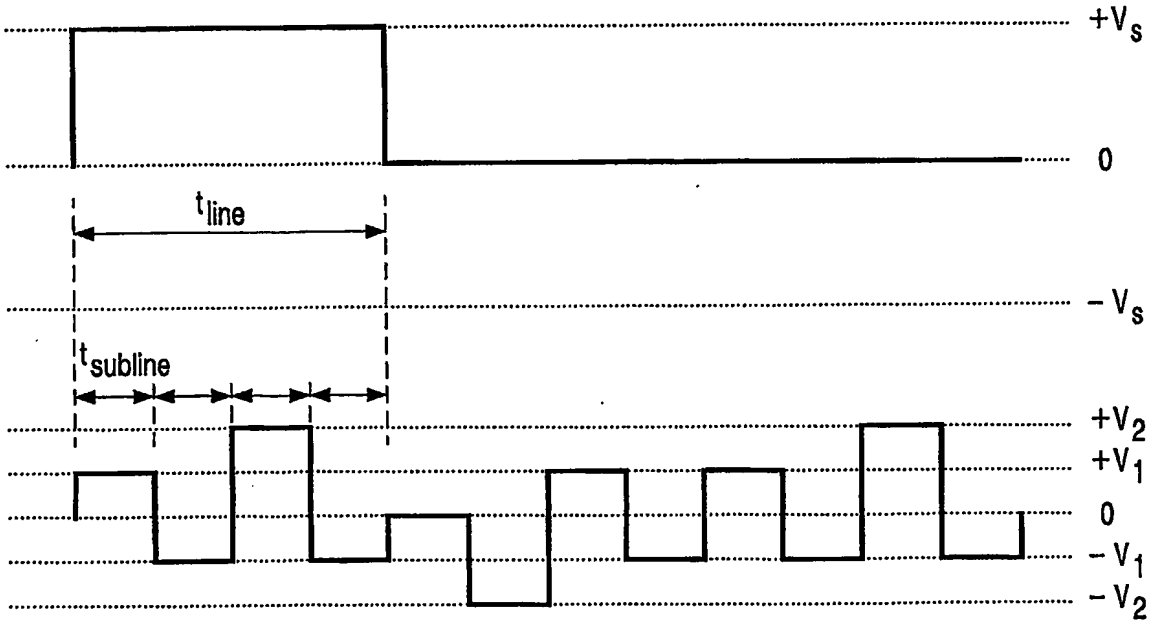

FIG. 2

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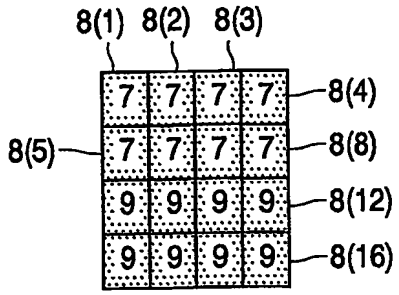

FIG. 3

frame 0				frame 1				----	frame 15			
0	5	13	11	1	6	14	12	----	15	4	12	10
4	10	2	7	5	11	3	8	----	3	9	1	6
0	5	13	11	1	6	14	12	----	15	4	12	10
4	10	2	7	5	11	3	8	----	3	9	1	6

FIG. 4

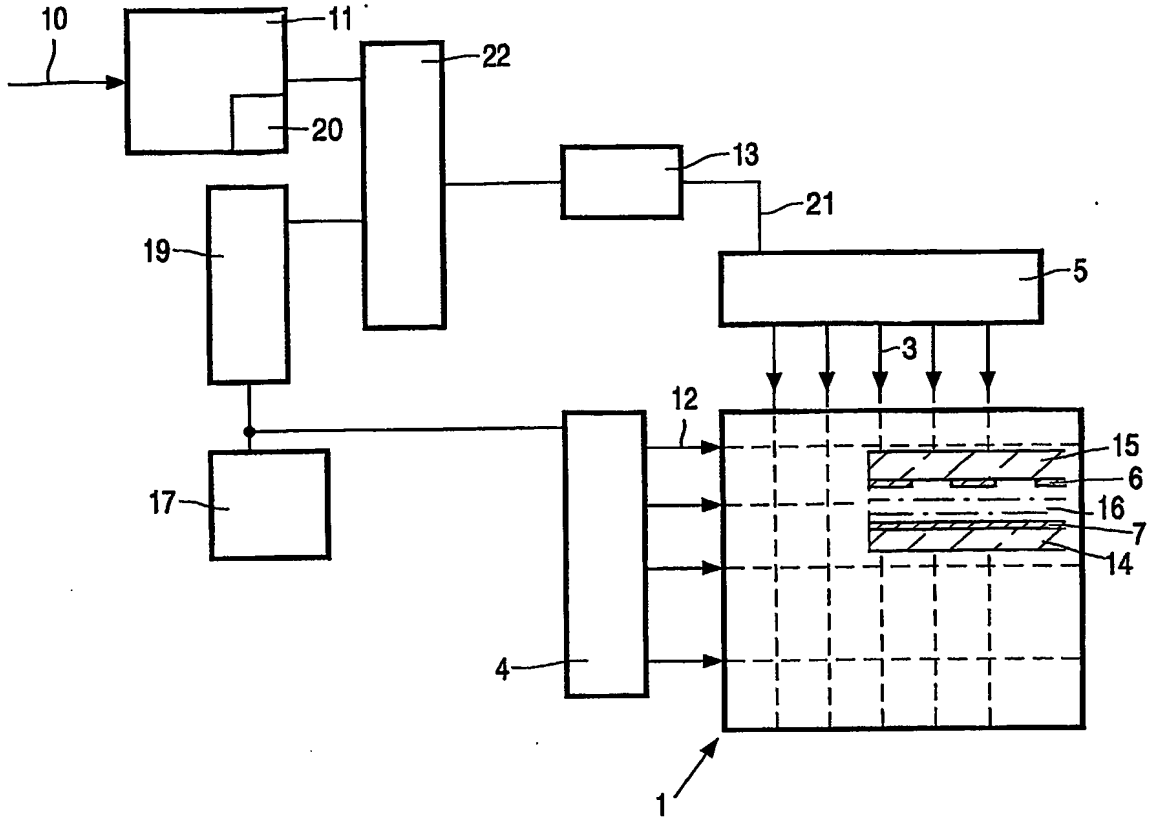
10
11
22
20
13
21
19
5
3
12
15
6
16
7
14
17
4
1

FIG. 5

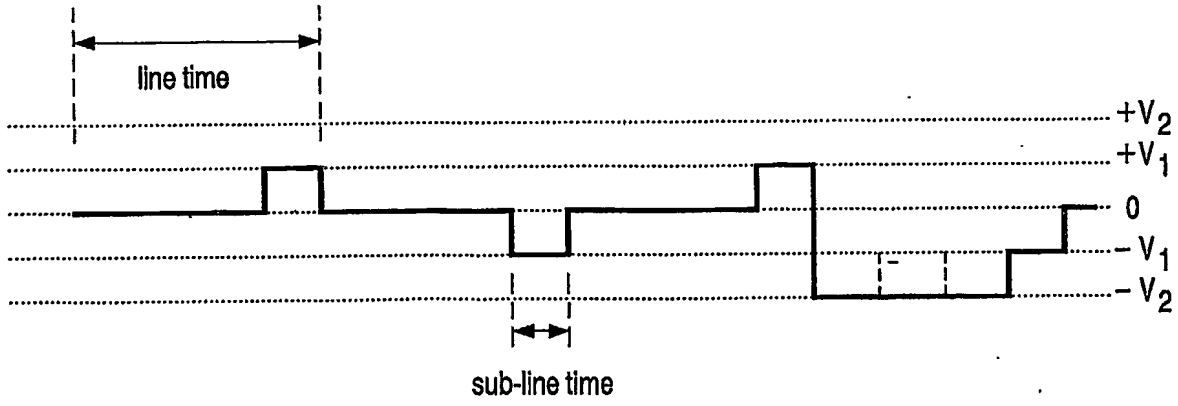
line time
+V2
+V1
0
-V1
-V2
sub-line time

FIG. 7

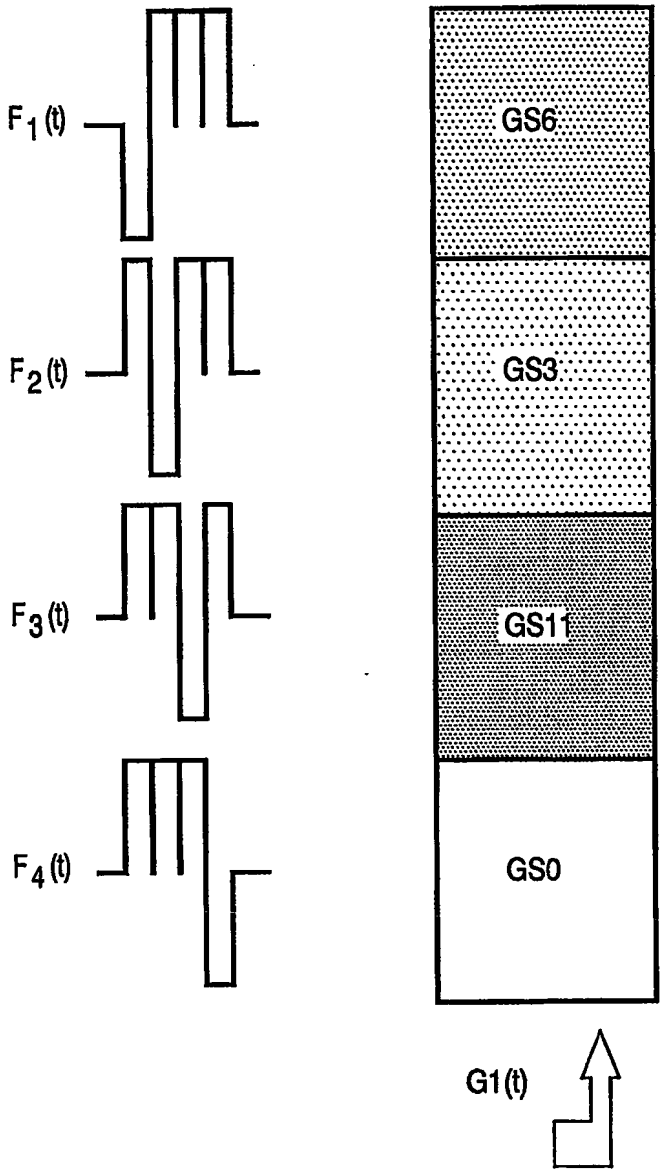

FIG. 6

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